IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A processor, comprising:

a processor core for executing an instruction in a pipeline processing;

a data memory accessed by said processor core; and

an extended arithmetic unit, connected to an exterior of said processor core, for processing ~~a particular~~ an extended instruction decoded in said processor core in the pipeline processing,

said extended arithmetic unit executing an arithmetic operation by using arithmetic operation data retained in a register file in said processor core, and outputting a result of an arithmetic operation directly to a memory stage processing in said processor core,

said processor core ~~saving~~ receiving the result of the arithmetic operation executed by said extended arithmetic unit and inputted therefrom ~~in~~ into said register file in said processor core, wherein said processor core includes a pipeline controller for flushing or stopping the pipeline processing in said extended arithmetic unit.

2. (Currently Amended) A processor, comprising:

a processor core for executing an instruction in a pipeline processing;

a data memory accessed by said processor core; and

an extended arithmetic unit, connected to an exterior of said processor core, for processing ~~a particular~~ an extended instruction decoded in said processor core in the pipeline processing,

said processor core, at least including:

an instruction memory for storing an instruction to be executed;

an instruction decode unit for reading out an instruction from said instruction memory to decode the instruction, in case that the instruction decoded is an extended ~~arithmetic unit control~~ instruction that should be executed by said extended arithmetic unit connected to the exterior of said processor core, said instruction decode unit also outputting at least an instruction code of said extended ~~arithmetic unit control~~ instruction to said extended arithmetic unit;

a register file for retaining arithmetic operation data of an arithmetic operation that should be executed by the instruction decoded, in case that said arithmetic operation data is data of said extended ~~arithmetic unit control~~ instruction, said register file also outputting said arithmetic operation data to said extended arithmetic unit;

a first operational section for executing the instruction decoded;

a pipeline controller for flushing or stopping the pipeline processing in said extended arithmetic unit, and

an extended arithmetic unit, at least including,

a second operational section for executing an arithmetic operation specified by said extended ~~arithmetic unit control~~ instruction by using said arithmetic operation data retained in said register file, and outputting an execution result of the arithmetic operation directly to a memory stage processing in said processor core.

3. (Currently Amended) The processor according to Claim 1, wherein,

in case that the instruction decoded is said extended ~~arithmetic unit control~~ instruction, said processor core outputs to said extended arithmetic unit at least an instruction

code that specifies an action involved in an arithmetic operation in said extended arithmetic unit and an instruction valid signal that indicates said instruction code is valid.

4. (Currently Amended) The processor according to Claim 1, wherein said arithmetic operation data outputted to said extended arithmetic unit is a value read out from said register file in said processor core in accordance with a register number specified by a part of said extended ~~arithmetic unit control~~ instruction.

5. (Currently Amended) The processor according to Claim 1, wherein said ~~processor core includes a~~ pipeline ~~control unit for controlling~~ controller ~~for controlling~~ controls pipeline processing in an interior of said processor core and in said extended arithmetic unit.

6.(Currently Amended) The processor according to Claim ~~5,~~ 1, wherein said pipeline ~~control unit~~ controller outputs to said extended arithmetic unit a first pipeline stop signal for ~~suspending execution of an instruction~~ stopping the pipeline processing in said extended arithmetic unit.

7. (Currently Amended) The processor according to Claim ~~5,~~ 1, wherein said pipeline ~~control unit~~ controller, in case that the instruction decoded is a jump instruction, outputs to said extended arithmetic unit a pipeline flush signal for ~~abandoning execution of an instruction outputted to~~ flushing a register in said extended arithmetic unit.

8. (Currently Amended) The processor according to Claim ~~5,~~ 1, wherein ~~said pipeline control unit stops execution of an instruction in said processor core in accordance with a~~

~~second pipeline stop signal for suspending execution of an instruction inputted from said extended arithmetic unit and executed by said processor core~~ said extended arithmetic unit further comprises a second pipeline controller for, in case that the extended instruction requires more than one cycle, asserting a second pipeline stop signal for stopping the pipeline processing in said processor core.

9. (Original) The processor according to Claim 1, wherein said extended arithmetic unit outputs to said processor core an arithmetic operation result invalidating signal that invalidates an execution result of an arithmetic operation executed in said processor core.

10. (Currently Amended) The processor according to Claim 1, wherein said ~~data memory~~ extended arithmetic unit comprises:

~~receives from said extended arithmetic unit at least one of an address for memory access, data, a write control signal for controlling data writing, and a read control signal for controlling data reading;~~

~~reads out the data from a region specified by said address and outputs the data to said extended arithmetic unit in case that data reading is carried out because said read control signal is asserted; and~~

~~writes the data inputted from said extended arithmetic unit into a region specified by said address in case that data writing is carried out because said write control signal is asserted~~

a first stage arithmetic circuit;

a second stage arithmetic circuit; and

a memory access controller configured to control direct access of said data memory by the extended arithmetic unit after an execution of the arithmetic operation by said first stage arithmetic circuit, and to provide said second stage arithmetic circuit with read out data from said data memory as input data for succeeding pipeline processing.

11. (Currently Amended) The processor according to Claim 1, wherein said extended arithmetic unit includes:

a plurality of pipeline-structured arithmetic circuits;

a first pipeline register for storing a processing result by an arithmetic circuit in a preceding stage at a rising of a following clock; and

a second pipeline register for storing a processing result by an arithmetic circuit in a succeeding stage at the rising of the following clock.

12. (Currently Amended) A processor core, connected to an extended arithmetic unit for processing an extended instruction decoded in said processor core in pipeline processing, and for ~~processing a particular~~ executing an instruction ~~to an exterior thereof,~~ in a pipeline processing, comprising:

an instruction memory for storing an instruction to be executed;

an instruction decode unit for reading out an instruction from said instruction memory to decode the instruction, in case that the instruction decoded is an extended ~~arithmetic unit control~~ instruction that should be executed by said arithmetic unit connected to the exterior of said processor core, said instruction decode unit also outputting at least an instruction code of said extended ~~arithmetic unit control~~ instruction to said extended arithmetic unit; and

a register file for retaining arithmetic operation data of an arithmetic operation that should be executed by the instruction decoded, and in case that said arithmetic operation data is data for said extended ~~arithmetic unit control~~ instruction, said register file also outputting said arithmetic operation data to said extended arithmetic unit, ~~and~~ storing a result of an arithmetic operation executed in said extended arithmetic unit, and outputted directly to a memory stage processing in said processor core;

a first operational section for executing the instruction decoded; and

a pipeline controller for flushing or stopping the pipeline processing in said extended arithmetic unit.

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13. (Currently Amended) The processor core according to Claim 12, wherein in case that the instruction decoded is said extended ~~arithmetic unit control~~ instruction, said instruction decode unit outputs to said extended arithmetic unit at least an instruction code that specifies an action involved in an arithmetic operation by said extended arithmetic unit and an instruction valid signal that indicates said instruction code is valid.

14. (Currently Amended) The processor core according to claim 12, wherein said arithmetic operation data outputted to said extended arithmetic unit is a value read out from said register file in said processor core in accordance with a register number specified by a part of said extended ~~arithmetic unit control~~ instruction.

15. The processor core according to claim 12, ~~further comprising~~ wherein ~~a~~ said pipeline ~~control unit for controlling~~ controller controls pipeline processing in an ~~internal~~ interior of said processor core and in said extended arithmetic unit.

16. (Currently Amended) The processor core according to claim 15, wherein said pipeline ~~control unit~~ controller outputs to said extended arithmetic unit a first pipeline stop signal for ~~suspending execution of an instruction~~ stopping the pipeline processing in said extended arithmetic unit.

17. (Currently Amended) The processor core according to claim 15, wherein said pipeline ~~control unit~~ controller, in case that the instruction decoded is a jump instruction, outputs to said extended arithmetic unit a pipeline flush signal for ~~abandoning execution of an instruction outputted to~~ flushing a register in said extended arithmetic unit.

18. (Currently Amended) The processor core according to claim 15, wherein said pipeline ~~control unit~~ controller stops execution of an instruction in said processor core in accordance with a second pipeline stop signal, ~~inputted from~~ asserted by said extended arithmetic unit in case that the extended instruction requires more that one cycle, for ~~suspending execution of an instruction~~ stopping the pipeline processing in said processor core.

19. (Currently Amended) The processor core according to claim 15, wherein said pipeline control unit receives from said extended arithmetic unit an arithmetic operation result invalidating signal that invalidates an execution result of an arithmetic operation in said processor ~~core, and invalidates the execution result of the arithmetic operation in said processor~~ core.

20. (New) A processor, comprising:

a processor core having a register file and configured to execute an instruction in a pipeline processing;

a data memory accessed by said processor core;

an extended arithmetic unit connected to an exterior of said processor core and configured to process an extended instruction decoded in said processor core in the pipeline processing, to execute an arithmetic operation by using arithmetic operation data retained in a register file in said processor core, and to output a result of an arithmetic operation directly to a memory stage processing in said processor core;

said processor core configured to receive the result of the arithmetic operation executed by said extended arithmetic unit and to input the received result into said register file in said processor core;

said processor core comprising a pipeline controller configured to flush or stop the pipeline processing in said extended arithmetic unit; and

said extended arithmetic unit comprises,

a first stage arithmetic circuit,

a second stage arithmetic circuit, and

a memory access controller configured to control direct access of said data memory by the extended arithmetic unit after an execution of the arithmetic operation by said first stage arithmetic circuit, and to provide said second stage arithmetic circuit with read out data from said data memory as input data for succeeding pipeline processing.